Analysis and Design of A 30 MHz Resonant SEPIC Converter*

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***Abstract*—This paper presents the analysis and design of a resonant SEPIC converter operating at 30 MHz. With the conventional design method, tuning the amplitude and phase of the fundamental input voltage and current affect each other so that the design procedure is trial-and-error. An improved design method is proposed by re-dividing the resonant SEPIC topology and defining the new variables to realize the independent tuning of the amplitude and phase. The loss analysis is provided. A 15 V input, 14 W/ 28 V output, 30 MHz prototype has been built to verify the proposed design method. The prototype achieves the efficiency above 80% over a wide load. Furthermore, a novel structure of the PCB embedded inductors is used in a 25 W prototype to further improve the power density.**

***Keywords*—VHF SEPIC; design method; PCB inductor**

I. Introduction

Modern power electronics applications expect power converters to have greater compactness, higher power density and higher efficiency. Therefore, increasing the switching frequency is an effective way to reduce the energy storage requirement, thus permitting use of smaller passive components and paving the way toward fully integrated power converters. Recently, the topic of the power converters operating at Very High Frequencies (VHF, 30-300 MHz) attracts a lot of research efforts [1].

For VHF power conversion, some important considerations impose requirements on circuit topologies. Firstly, owing to the extreme high switching frequency, the parasitic capacitance and inductance can not be neglected. In this case, the topologies which can effectively absorb device capacitance and parasitic inductance as part of their operation have become a priority to be dealt with. Secondly, pushing frequency upwards means the loss in the semiconductor device increases significantly. Therefore, maintaining high efficiency at increased operation frequency is so important that soft switching should be taken into consideration at the meantime. To be effective at such high frequencies, a circuit topology should have both of these characteristics to some degree. Furthermore, the practicality of driving the active switches is related to the circuit topologies for VHF operation. The switch control ports referenced to the "flying" circuit node are ill-suited to extreme high frequencies at present because the reliability of the driving circuit has not been demonstrated. Consequently, the circuit topologies having the ground-referenced active switches are generally preferred at VHF.

Based on the compactness of the circuit topologies, VHF resonant boost converter [2] and VHF resonant SEPIC converter [3] are two non-isolated circuit with minimum components. Compared with the VHF resonant boost converter, the VHF SEPIC converter has the ability to provide buck and boost power conversion so that this topology has a broader range of applications [4].

However, the design method of the VHF converters is more difficult than the conventional PWM converters. This is because that there is a multi-resonant procedure in the mode analysis and therefore, the numerical solutions of the components are hard to be obtained. The convenient design method using simulation for the resonant boost converter has been used. Compared to the resonant boost converter, the resonant SEPIC converter has an additional resonant capacitance, which makes the operation mode involve a five order resonant network. So the design is more complicated.

This paper introduces a 30 MHz resonant SEPIC converter and proposes a design method maintaining high efficiency. In addition, a new structure of PCB inductors is proposed to further improve the power density.

II. Conventional Design Method For Resonant Sepic Converter

A VHF DC-DC converter topology typically comprises a resonant inverter coupled to a resonant rectifier as illustrated in Fig.1. In some case, the matching network interconnecting the two is used to provide some combination of filtering, isolation and voltage transformation (via a transformer [5]). However, the matching network may increase the complexity of the circuit topology and design method and even reduce power conversion efficiency.

The resonant SEPIC converter is shown in Fig.2. In [4], the resonant SEPIC topology is understood as the combination of an inverter stage, a rectifier stage and a matching network shown in Fig.3. Normally, the conventional design method involves four steps: 1) tune the rectifier stage; 2) design the matching network; 3) design the inverter stage; 4) dc-dc returning. However, the drawbacks of the conventional design method include:

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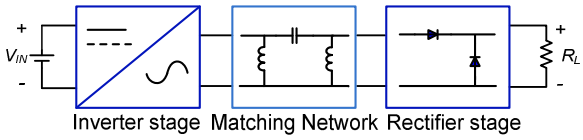


Fig.1 Structure of a typical VHF DC-DC converter

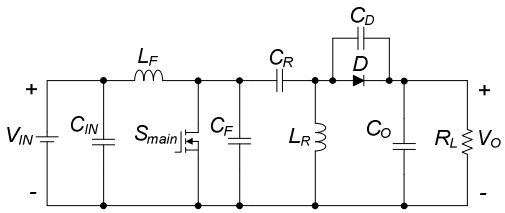


Fig.2 A VHF resonant SEPIC topology

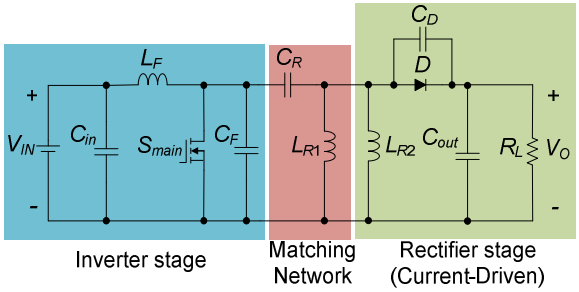


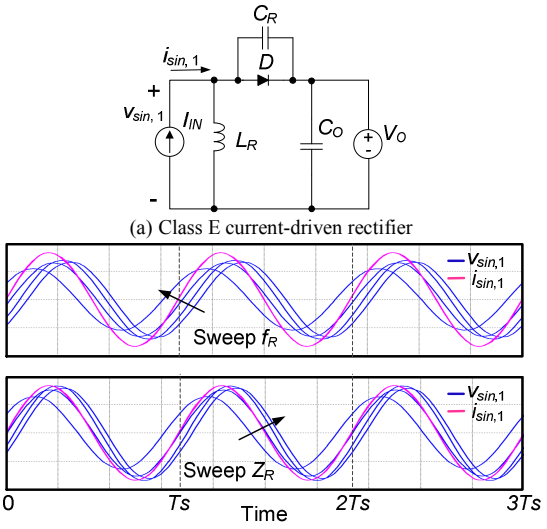
Fig.3 Three subsystems of the resonant SEPIC topology

1) The difficulty of determining the proper amplitude of the current source injected into the rectifier stage

The first step, design of the rectifier stage, is the most important, because the equivalent resistance used instead of the rectifier stage will impact next design procedure. The rectifier stage is a class E current-driven rectifier as shown in Fig.4(a) [6]. It is assumed that the majority of the output power is delivered through the fundamental component so that the rectifier is driven by a sinusoidal current source of amplitude I_{IN}. When tuning the rectifier design, the amplitude I_{IN} should be assumed first. However, different I_{IN} results in different values of L_R and C_R for the same purpose that the rectifier appears resistive based on the same output level. So this causes the problem to select the proper amplitude I_{IN} and choose the right parameters of the rectifier.

2) The complexity of the tuning method of the rectifier stage

The design method of the class E current-driven rectifier topology in the resonant SEPIC converter in Fig.4(a) is defining a resonant frequency f_R and characteristic impedance Z_R and tuning the values in turn. f_R (defined as $f_R = 1/2\pi\sqrt{L_R C_R}$) and Z_R (defined as $Z_R = \sqrt{L_R / C_R}$) are used to establish resistive operation at a given input and output voltage and satisfy the output power requirement. Fig.4(b) shows the fundamental waveforms of the simulated input rectifier voltage $v_{sin,\,1}$ and current $i_{sin,\,1}$. As f_R is swept, the phase angle between $v_{sin,\,1}$ and $i_{sin,\,1}$ changes. While f_R makes the rectifier look like a resistance at the switching frequency, sweeping the value of Z_R not only changes the input fundamental current amplitude but also changes the phase angle between $v_{sin,\,1}$ and $i_{sin,\,1}$. Therefore, the design procedure needs a lot of iterations.



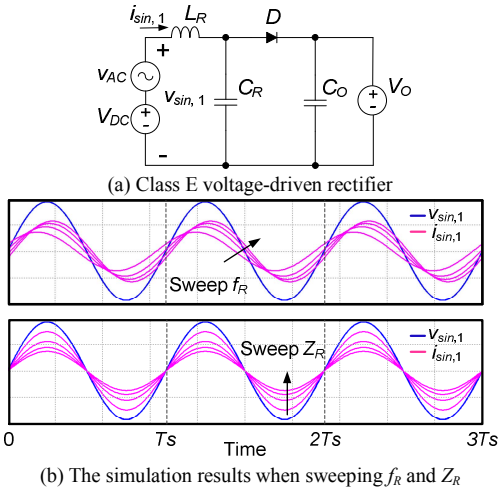
(a) Class E current-driven rectifier

(b) The simulation results when sweeping f_R and Z_R

Fig.4 Design of the Class E current-driven rectifier for the resonant SEPIC converter

Compared with the rectifier analyzed above, a convenient approach in [7] is proposed to select the component values of the class E voltage-driven rectifier in the resonant boost topology as shown in Fig.5(a). It is noted that the parasitic capacitance of the diode is absorbed by the resonant capacitance C_R. Based on the same definition of f_R and Z_R, it can be found that sweeping f_R changes the phase angle between $v_{sin,\,1}$ and $i_{sin,\,1}$, while sweeping Z_R only affects the amplitude of $i_{sin,\,1}$, but not the phase angle in Fig.5(b).

In general, the formulation in the class E voltage-driven rectifier is approximately orthogonal permitting to tune the rectifier by sweeping f_R followed by Z_R easily. The ability to control these parameters independently allows easy design. However, f_R and Z_R are dependent on each other in the class E current-driven rectifier so that the design procedure becomes more complex. With the two considerations above in mind, the design of the rectifier stage in the resonant SEPIC converter becomes of difficulty.



(a) Class E voltage-driven rectifier

(b) The simulation results when sweeping f_R and Z_R

Fig.5 Design of the Class E voltage-driven rectifier for the resonant boost converter

3) The trial-and-error design of the matching network and inverter stage

The matching network that is used to provide a transformation ratio is designed individually based on the equivalent impedance of the rectifier stage. This increases the complicacy and inaccuracy of the total design procedure. Furthermore, the design of the matching network and the inverter stage is coupled seriously.

Based on the above analysis, the above three drawbacks of the conventional approach make it difficult design the resonant SEPIC converter effectively and efficiently.

III. Proposed Design Method For Resonant Sepic Converter

A. Proposed Design Method

To simplify the design method of the resonant SEPIC topology, it is re-divided into a class Φ inverter and a class E voltage-driven rectifier with a series capacitor shown in Fig.6. Therefore, the design method for this topology involves three steps: 1) design the rectifier; 2) design the inverter; 3) dc/dc returning.

1) Design of The Rectifier Stage

Comparing with the class E rectifier in the resonant boost topology in Fig.5(a), the one in the resonant SEPIC topology is shown in Fig.7. It is noted that the difference between the two is the change in the location of the resonant inductance L_R and resonant capacitance C_R. However, the capacitance C_R and C_D are not equivalent so that this rectifier has three resonant components.

The design method of the resonant SEPIC converter starts with the rectifier stage. For the rectifier stage, the design criterion includes: a) the duty ratio of the rectifier diode is around 0.5 for the trade-off of the current and voltage stress; b) the fundamental component of the input voltage and current of the rectifier are in phase for the efficiency optimization; c) the desired power transmission is achieved.

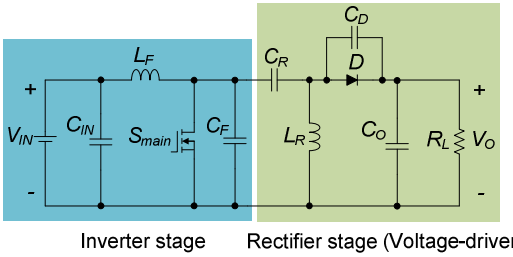


Fig.6 Two subsystems of the resonant SEPIC topology

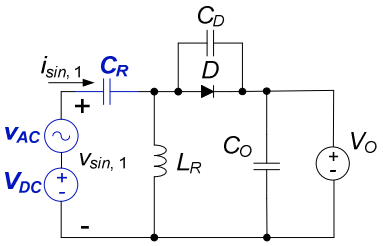


Fig.7 Class E voltage-driven rectifier with a series capacitor

To achieve the above rules, a simulation model is built shown in Fig.7. Assuming that ideally all the power is delivered with the fundamental component, the input voltage of the rectifier can be modeled as a sinusoidal voltage v_{AC} on the assumption that the amplitude is $(4V_{IN})/\pi$ and a dc component V_{DC} equal to V_{IN} [7]. $v_{sin,1}$ and $i_{sin,1}$ are the fundamental input voltage and current. The load is modeled by a dc voltage source V_O.

Because there are three resonant components, the method to select the values of L_R, C_R and C_D begins with defining three variables: the resonant frequency f_R, the characteristic impedance Z_R and the scaling factor k.

$$f_R = \frac{1}{2\pi\sqrt{L_R(C_R + C_D)}} \tag{1}$$

$$Z_R = \sqrt{\frac{L_R}{C_R + C_D}} \tag{2}$$

$$k = \frac{C_R}{C_D} \tag{3}$$

The scaling factor k is selected first. The initial value of k is selected as $k = V_o/V_{IN}$. Then f_R is swept until $v_{sin,1}$ and $i_{sin,1}$ are in phase. Once k and f_R are decided, the duty ratio of the diode is determined. If the duty cycle is too high or too low, the value of k should be re-selected. The duty ratio increases with k. Third, Z_R is swept with k and f_R kept constant until the desired output power is achieved as shown in Fig.8. It is noted that the resonant capacitance C_D should be higher than the parasitic capacitance of the diode. At last the impedance from the input port of the rectifier appears resistive at the fundamental frequency and this equivalent resistance R_{rec} can be derived as (4). η is the assuming efficiency of the rectifier stage.

$$R_{rec} = \frac{8\eta}{\pi^2} \cdot \frac{V_{IN}^2}{P_{OUT}} \tag{4}$$

2) Design of The Inverter Stage

The rules to design the inverter stage include: a) achieve ZVS for the power MOSFET; b) realize efficient power conversion.

The component design in the inverter stage is based on the impedance characteristic at the MOSFET output port when the switch is off (Z_{DS}). Fig.9 gives the equivalent circuit across the MOSFET. The rectifier stage is replaced with the equivalent resistance R_{rec}.

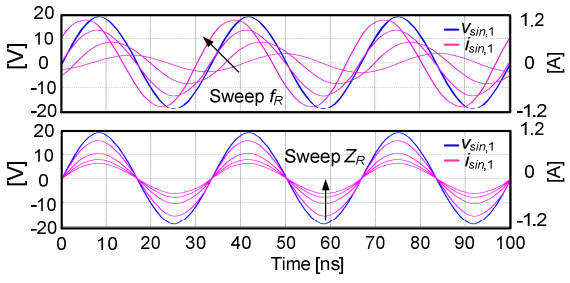


Fig.8 The fundamental component of the rectifier input voltage and current when sweeping f_r and Z_o

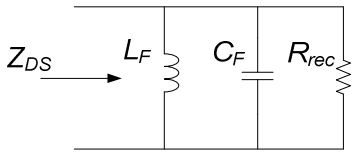


Fig.9 Equivalent impedance at the switch output port

To achieve ZVS of the MOSFET, the phase angle of the impedance Z_{DS} at the fundamental of the switching frequency is 30° - 60° inductive [8]. The resonant frequency of the inductor L_F and the capacitance C_F, the ratio A about the switching frequency f_S and the resonant frequency f_F are defined as (5), (6). Then the relationship between the ratio A and phase angle θ is illustrated as (7).

$$f_F = \frac{1}{2\pi\sqrt{L_F C_F}} \tag{5}$$

$$A = \frac{f_S^2}{f_F^2} \tag{6}$$

$$A = \frac{C_F \cdot (2\pi f_S) \cdot R_{rec}}{C_F \cdot (2\pi f_S) \cdot R_{rec} + \tan(\theta)} \tag{7}$$

A good starting point is assuming C_F is entirely provided by the switch and θ is 45°. Based on (5), (6) and (7), L_F can be decided. Then delivered power should be simulated to confirm if it exceeds the output power. If the inverter can not provide enough power, the C_F should be re-selected.

3) dc-dc retuning

An entire converter design may be accomplished by connecting the tuned inverter to the rectifier. The circuit waveforms and the output power level may be slightly different due to the non-linear interaction between the two stages. Fine additional tuning may thus be required by choosing the new value of the phase angle θ to achieve ZVS and the required power level.

B. Comparison and Benefits of Proposed Design Method

The resonant SEPIC converter is re-divided into two subsystems so that the phase between the fundamental input voltage and current, and the amplitude of the fundamental input current can be tuning independently when designing the rectifier. Furthermore, the voltage source (V_{DC} and v_{AC}) applied to the rectifier and the equivalent impedance of the rectifier (R_{rec}) are only determined by the specifications of the converter, (i.e. V_{IN}, V_O, P_O) other than the circuit component values. So the design procedure of the rectifier and inverter stage is decoupled.

C. Loss Analysis

The majority of the power loss in the resonant SEPIC converter includes:

1) The conduction loss and gate drive loss of the power MOSFET S_{main} are expressed by (8) and (9).

$$P_{ON} = I_{rms}^2 \cdot R_{DS,on} \tag{8}$$

$$P_{GATE} = I_{R_g}^2 \cdot R_g \tag{9}$$

Note that I_{rms} and I_{Rg} are the RMS current through the MOSFET and the R_g of the MOSFET. In addition, $R_{ds,on}$ and R_g are the drain-source on-state resistance and gate resistance which can be obtained from the datasheet of the chosen MOSFET.

2) The conduction loss of the diode D is expressed as

$$P_D = I_F \cdot V_F \tag{10}$$

where I_F is the average current through the diode and V_F is the forward voltage drop.

3) The loss in inductor L_F and L_R that can be expressed as

$$P_{Inductor} = I_{dc,rms}^2 \cdot R_{dc} + I_{ac,rms}^2 \cdot R_{ac} \tag{11}$$

The loss in the inductors contains dc loss and ac loss. In VHF applications, ac loss becomes more important so that it should be estimated. Generally, the fundamental component is the dominant and it may cause main loss. Therefore, $I_{ac,rms}$ is the fundamental RMS current obtained by simulating and R_{ac} is the fundamental impedance that is calculated by the Q factor at the fundamental frequency in the datasheet.

Using the proposed design method, the component values obtained are given in Table I. The specifications of the first converter are 30 MHz switching frequency, 15 VDC input, 14 W/28 VDC output. The commercial Si MOSFET from Vishay is used as the power switch for low cost. Note that the capacitance C_F uses the parasitic output capacitance of the MOSFET only.

The calculated loss breakdown is given in Table II. The estimated efficiency of the converter is about 85% and the loss distribution is given in Fig.10.

TABLE I POWER STAGE COMPONENT VALUES

L_F	33 nH	C_F	300 pF
L_R	68 nH	C_R	300 pF
		C_D	150 pF
C_{in}	30 µF	C_{out}	60 µF
S_{main}	SI7454DDP (Vishay)	D	STPS1H100 (ST) × 2

TABLE II LOSS BREAKDOWN

Conduction Loss(S_{main})	0.215 W
Gate Drive Loss	0.713 W
Conduction Loss (D)	0.331 W
Inductor L_F	0.425 W
Inductor L_R	0.782 W
Total Loss	2.466 W

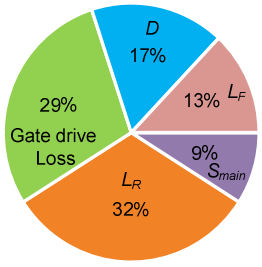


Fig.10 Loss Distribution:
V_{in} = 15 V, V_o = 28 V, f_s=30 MHz

IV. Proposed Structure Of Multi-Layer Solenoid Inductors

To further improve the power density, the inductors should be optimized. The PCB inductors, especially the planar spirals have become essential elements of the communication circuit blocks. In VHF applications, the inductors have the same magnitude so that the PCB inductors can also be used. However, the structure is more significant because the current through the inductors is larger and ac loss may increase significantly.

Planar inductors, such as the square spirals, the circular spirals, are the basic because of the simple structure and the ease of their layout. Moreover, accurate expressions have been obtained which makes the inductor design become convenience. Among them, the structure of the square spiral inductors shown in Fig.11 is the most popular [9].

In addition, the PCB embedded inductors have been used in VHF Switch-Mode Power Supplies (SMPS) [10]. In [11], the prototype with the solenoid inductors gives a power density of 146 W/inch^3. However, this structure results in the series resistance of the PCB inductors are a bit higher than the discrete parts which causes the efficiency to drop 4 percent. That is to say, the PCB embedded inductors can push the power density effectively. But the structure is the key point to determine the series resistance and loss to some extent.

To fully take advantage of the multi-layer PCB, a novel structure of the multi-layer solenoid PCB embedded inductors is proposed. In this work, a four-layer solenoid inductor has been adopted. The structure shown as Fig.12 is that each layer has only one turn and one layer connects another by holes. It utilizes four layers to improve the power density and adjusts the inside and outside diameters to get the proper value and the ac resistance.

To verify this structure, the 3D model is built. It's important to note that the copper thickness of PCB inductors is 2 oz based on a tradeoff between the cost and the resistance. The comparison of the three, the discrete inductor from Coilcraft, the planar spiral inductor and the four-layer solenoid PCB embedded inductor, is given in Table III. It can be found that the four-layer solenoid PCB embedded inductors not only have the smallest volume, but also have the smallest series resistance.

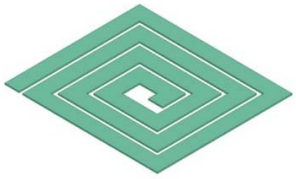


Fig.11 Structure of the planar spiral inductors

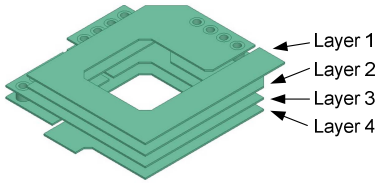


Fig.12 The structure of the four-layer solenoid PCB embedded inductors

Table III The comparison among three kinds of inductors

Structure	Discrete	Planar Spiral	Four-layer Solenoid
L/nH	68	66.79	68.38
Size/mm×mm×mm	7×5×5	12×9×1.6	7×7×1.6
R_{AC}@ 30 MHz/mΩ	142	290.27	114.32

A four-layer solenoid PCB embedded inductor is designed to instead the rectifier inductor L_R because of its size. The experimental results about the second 15 V to 28 V, 25 W resonant SEPIC converter are given in the next section.

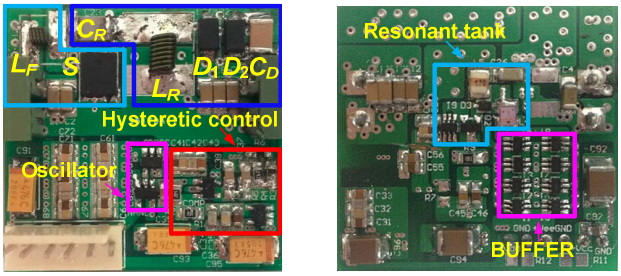
V. Experimental Results And Discussion

A. The first prototype with the discrete inductors

In order to verify the proposed design method, the first resonant SEPIC converter prototype shown in Fig.13 is built.

The multi-stage resonant gate driver is used in this converter [12]. The gate drive voltage v_{GATE} and the drain to source voltage of the MOSFET v_{DS} are shown in Fig.14. v_{GATE} has a 2.5 V dc offset close to the threshold voltage of the power MOSFET and the duty ratio is about 0.5. From the waveform of v_{DS}, it is noted that ZVS is achieved.

Fig.15 shows the anode voltage of the rectifier diode to ground. The peak reverse voltage of the diode nears 90 V. The duty cycle of the diode is about 0.3.



(a) Top (b) Bottom

Fig.13 Photo of prototype (39 mm × 37 mm)

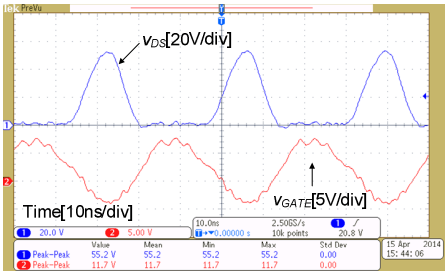


Fig.14 The waveforms of v_{DS}, v_{GATE} at 15V input

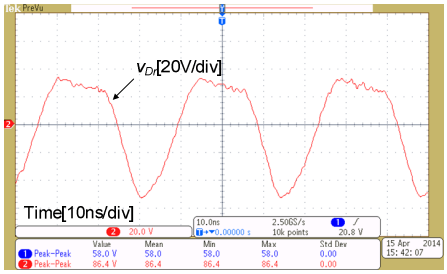


Fig.15 Measured anode voltages of the rectifier diode

The hysteretic control is applied to realize close loop. The entire converter is modulated to be on and off at a frequency in the range of 80 KHz - 300 KHz far below the switching frequency. Fig.16 shows the close-loop efficiency at the nominal input voltage of 15V. At full load, the converter outputs 14 W with an efficiency of 82.5%. Below 4.2 W, the efficiency tends to decrease when the load increases. This is because the gate drive loss increases dramatically as the modulation frequency increases with the load increases. Then the gate drive loss slightly increases and the loss of power components is the dominant part. Fig.17 shows the efficiency when the input voltage changes.

The thermal imaging of the prototype is shown in Fig.18 that demonstrates the loss of the rectifier inductor L_R is high.

B. The second prototype with the PCB inductors

For the objective of further increasing power density, a resonant SPEIC DC-DC converter with the proposed four-layer solenoid PCB embedded inductor has been built. The prototype is shown in Fig.19.

The waveforms of this converter are similar to the last. The converter outputs 25 W with the efficiency of 82% and the power density is over 200 W/inch^3.

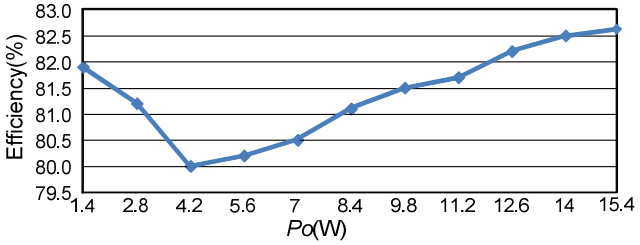


Fig.16 Close-loop efficiency for V_{IN}=15 V, V_O=28 V

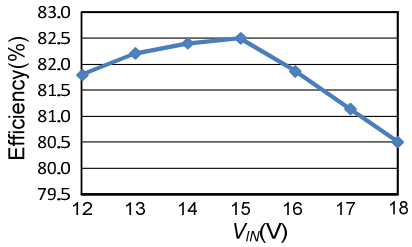


Fig.17 Close-loop efficiency for P_O=14 W

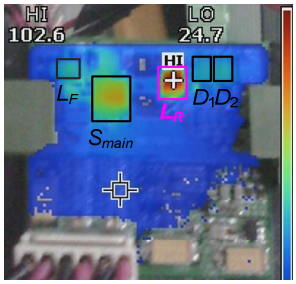
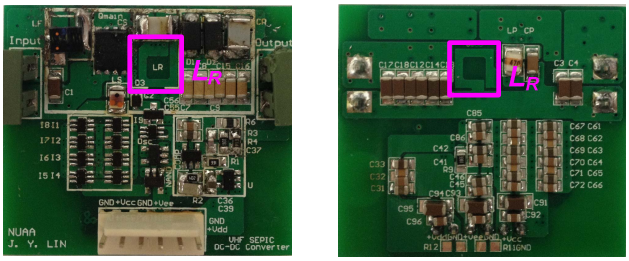


Fig.18 Thermal imaging of the prototype for P_O=14 W



(a) top (b) bottom

Fig.19 Photo of prototype

VI. Conclusion

A VHF resonant SEPIC converter is introduced and a design method for the converter is proposed. The conventional design method has the problem that the amplitude and phase of the fundamental input voltage and current affect each other. Therefore, the design procedure is trial-and-error. The proposed design method solves this problem by re-dividing the converter and defining new variables. This paper demonstrates two experimental prototypes. The first one with the discrete inductors outputs 14 W and achieves the efficiency above 80% in wide load range. The second one uses the four-layer solenoid PCB embedded inductors with the power density over 200 W/inch^3.

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